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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/812,056	03/30/2004	Masahiro Ito	Q80548	1303

23373 7590 11/16/2009

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EXAMINER	
SITTA, GRANT	

ART UNIT	PAPER NUMBER
2629	

NOTIFICATION DATE	DELIVERY MODE
11/16/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/812,056	ITO ET AL.	
	Examiner	Art Unit	
	GRANT D. SITTA	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 August 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9* is/are allowed.

6)☒ Claim(s) *1-5,7-8,10-23* is/are rejected.

7)☒ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 20 and 22 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 20 and 22. (new) the video processor of claim 1, wherein said bit rate converter compares said total value with a random variable threshold and performs said selection pending on a result of the comparison. Examiner was unable to locate in the specification wherein the bit rate converter compares said total value with a random variable threshold.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1, 3-4, 10-20, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Atsushi (JP Publication number 2002-221950) hereinafter Atsushi in view of Kitagawa et al (2002/0063784) hereinafter, Kitagawa further in view of Juri et al (5,329,475) hereinafter, Juri

4. In regards to claim 1, Atsushi teaches a video processor comprsing: a bit rate converter for converting (fig. 1 (10)) an M-bit input (fig. Input into 10) video signal to an N-bit (fig. 1 output of 10) output video signal by retaining grayscale levels (0068-0071), wherein N is smaller than M (0071); and

a pseudo-tone processing means (fig. 1 (11)) and frame memory (fig. 1 (10)), when said N-bit output (0086) video signal of said bit rate converter (fig. 1 (10)) corresponds to one of the plurality of N-bit input grayscale levels (0071-0082)

said pseudo-tone processing means (fig. 1 (11)) and frame memory (fig. 1 (10)) delivering one of a plurality of K-bit output grayscale levels to said display device (fig. 1 (13 to 14)).

Atsushi fails to teach a gamma correction memory in which a plurality of N-bit input grayscale levels are mapped to a plurality of K-bit output grayscale levels which are distributed on a non-linear curve corresponding to a non-linear curve on which grayscale levels of a display device are distributed.

However, Kitagawa teaches a gamma correction memory (fig. 1 (13) [0030]) in which a plurality of N-bit input grayscale levels (fig. 1 (11 bits of 13) [0020]) are mapped (fig. 7 [0029]) to a plurality of K-bit output grayscale levels which are distributed ([0020) on a non-linear curve (fig. 7) corresponding to a non-linear curve on which grayscale levels ([0020 and 0029]) of a display device are distributed [0020].

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Atsushi to **substitute** the use of a gamma correction memory, for the memory (fig. 1 (10)) of Atsushi, as taught by Kitagawa in order to perform gamma correction in order to properly show shadow detail in RBG images and to avoid gradation deterioration in gray zones ([0005] of Kitagawa).

Atsushi and Kitagawa fail to expressly teach said bit rate converter summing a binary-1 to a least significant bit position of higher N bits of said M-bit input video signal; and

selecting, as said N-bit output video signal, the summed higher N bits or higher N bits of said M-bit input video signal depending on a total value of bits ranging from the (N+ 1)th significant position to the least significant position of said M-bit input video.

However, Juri teaches bit rate converter summing a binary-1 to a least significant bit position of higher N bits of said M-bit input video signal; and

selecting, as said N-bit output video signal, the summed higher N bits or higher N bits of said M-bit input video signal depending on a total value of bits ranging from the (N+ 1)th significant position to the least significant position of said M-bit input video (fig. 1 and 5,col. 2-3, lines 63-21 col. 4-5, lines 58-35).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Atsushi and Kitagawa to **include** the use of data round-off device, as taught by Juri in order to perform a round-off device in which quantizing error is attenuated, and efficiency is increased as stated in col. 1, l lines 64-67).

5. In regards to claim 17, Atsushi teaches a video processor comprising (abstract fig. 1):

a first component processor for processing a first component of an RGB color model (fig. 1 (10) R);

a second component processor for processing a second component of the RGB color model (fig. 1 (10) G); and

a third component processor for processing a third component of the RGB color model (fig. 1 (10) B), Examiner notes first that Applicant has not claimed wherein the component processors are separate and distinct and second from 0071 the component processing is carried out separately inside fig. 1 (10).

wherein each of the first, second and third components processor comprises:

a bit rate converter for converting (fig. 1 (10)) an M-bit input (fig. Input into 10) video signal to an N-bit (fig. 1 output of 10) output video signal by retaining grayscale levels (0068-0071), wherein N is smaller than M (0071); and

a pseudo-tone processing means (fig. 1 (11)) and frame memory (fig. 1 (10)), when said N-bit output (0086) video signal of said bit rate converter (fig. 1 (10)) corresponds to one of the plurality of N-bit input grayscale levels (0071-0082)

said pseudo-tone processing means (fig. 1 (11)) and frame memory (fig. 1 (10)) delivering one of a plurality of K-bit output grayscale levels to said display device (fig. 1 (13 to 14)).

Atsushi fails to teach a gamma correction memory in which a plurality of N-bit input grayscale levels are mapped to a plurality of K-bit output grayscale levels which are distributed on a non-linear curve corresponding to a non-linear curve on which grayscale levels of a display device are distributed.

However, Kitagawa teaches a gamma correction memory (fig. 1 (13) [0030]) in which a plurality of N-bit input grayscale levels (fig. 1 (11 bits of 13) [0020]) are mapped (fig. 7 [0029]) to a plurality of K-bit output grayscale levels which are distributed ([0020) on a non-linear curve (fig. 7) corresponding to a non-linear curve on which grayscale levels ([0020 and 0029]) of a display device are distributed [0020].

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Atsushi to **substitute** the use of a gamma correction memory, for the memory (fig. 1 (10)) of Atsushi, as taught by Kitagawa in order to perform gamma

correction in order to properly show shadow detail in RBG images and to avoid gradation deterioration in gray zones ([0005] of Kitagawa.

Atsushi and Kitagawa fail to expressly teach said bit rate converter summing a binary-1 to a least significant bit position of higher N bits of said M-bit input video signal; and

selecting, as said N-bit output video signal, the summed higher N bits or higher N bits of said M-bit input video signal depending on a total value of bits ranging from the (N+ 1)th significant position to the least significant position of said M-bit input video.

However, Juri teaches bit rate converter summing a binary-1 to a least significant bit position of higher N bits of said M-bit input video signal; and

selecting, as said N-bit output video signal, the summed higher N bits or higher N bits of said M-bit input video signal depending on a total value of bits ranging from the (N+ 1)th significant position to the least significant position of said M-bit input video (fig. 1 and 5,col. 2-3, lines 63-21 col. 4-5, lines 58-35).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Atsushi and Kitagawa to **include** the use of data round-off device, as taught by Juri in order to perform a round-off device in which quantizing error is attenuated, and efficiency is increased as stated in col. 1, l lines 64-67).

6. In regards to claim 3, Atsushi as modified by Kitagawa teaches wherein said K-bit (fig.1 (output to display of Atsushi) output grayscale ([0029] of Kitagawa) levels value, are interpolated grayscale ([0029] of Kitagawa) levels of the N-bit input (fig. 1 (reduced bits from 10) of Atsushi) grayscale levels ([0029] of Kitagawa). Examiner notes the interpolation is part of the non-linear gamma correction as taught by Kitagawa and the N-bits and K-bits are taught by Atsushi, since the gamma correction memory of Kitagawa was substituted.

7. In regards to claim 4, Atsushi teaches wherein K is equal to M (0082) and (fig. 1 (12)).

8. In regards to claim 10, Atsushi discloses wherein M is 18 bits (fig. 1 RGB 6:6:6) [0006-0007, 0077]).

Atsushi does not disclose expressly wherein M is 10.

At the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to make M equal to 10 bits because Applicant has not disclosed that wherein M is 10 provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with 18, 16, 12 or any other bit value depending on the input signal because the device may be given different input signals.

Therefore, it would have been obvious matter of design choice to modify Atsushi to obtain the invention as specified in claims [s].

9. In regards to claim 11, Atsushi discloses wherein N is 12 bits (fig. 1 RGB 6:6:6) [0006-0007, 0077]).

Atsushi does not disclose expressly wherein N is 8.

At the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to make N equal to 8 bits because Applicant has not disclosed that wherein N is 8 provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with 18, 16, 12 or any other bit value because using various values will determine the amount of memory saved.

Therefore, it would have been obvious matter of design choice to modify Atsushi to obtain the invention as specified in claims [s].

10. In regards to claim 12, Atsushi discloses wherein K is 18 bits (fig. 1 RGB 6:6:6) [0006-0007, 0077]).

Atsushi does not disclose expressly wherein K is 8.

At the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to make K equal to 8 bits because Applicant has not disclosed that wherein K is 8 provides an advantage, is used for a

particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with 18, 16, 12 or any other bit value because a table stores trans values and as Atsushi states "many bits can also be formed to other bit values" [0077] .

Therefore, it would have been obvious matter of design choice to modify Atsushi to obtain the invention as specified in claims [s]. Examiner also notes that claim 12 depends from claim 1 and do not require that M be 10 or N is 8 since claims 10 and 11 are separate dependent claims.

11. In regards to claim 13 Atsushi teaches the video processor of claim 1, wherein the M-bit input video signal corresponds to a first component of an RGB color model (abstract and fig 1 RGB input to 10).

12. In regards to claim 14, Atsushi teaches the video processor of claim 13, wherein the first component is a red component (fig. 1 R of RGB).

13. In regards to claim 15, Atsushi teaches the video processor of claim 13, wherein the bit rate converter converts the M-bit input video signal corresponding to the first component independent of signals corresponding to a second and a third component of the RGB color model (fig. 1 (RGB) [0071]).

14. In regards to claim 16. Atsushi teaches the video processor of claim 13, wherein the N-bit input grayscale levels correspond to the first component of an RGB color model [0074-0077]. Examiner notes that the N-bit input grayscales correspond to the first component R.

15. In regards to claim 18, Atsushi discloses wherein N is 12 bits (fig. 1 RGB 6:6:6) [0006-0007, 0077]).

Atsushi does not disclose expressly wherein N is 6.

At the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to make N equal to 6 bits because Applicant has not disclosed that wherein N is 8 provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with 18, 16, 12 or any other bit value because a table stores trans values and as Atsushi states "many bits can also be formed to other bit values" [0077] .

Therefore, it would have been obvious matter of design choice to modify Atsushi to obtain the invention as specified in claims [s].

16. In regards to claim 19, (new), Atsushi teaches the video processor of claim 1, wherein N is less than K.(fig. N is equal to 12 bits and the output of 12 is 18 bits).

17. In regards to claims 20 and 22, Atsushi and Kitagawa as modified by Juri teaches the video processor of claim 1, wherein said bit rate converter compares said total value with a random variable threshold and performs said selection pending on a result of the comparison (fig. 5 (23) Juri).

18. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Atsushi and Kitagawa and Juri further in view of Lumelsky et al (5,196,924) hereinafter, Lumelsky,

19. In regards to claim 2, Atsushi and Kitagawa discloses the limitations of claim 1,

Atsushi, Kitagawa and Juri differ from the claimed invention in that Atsushi does not disclose wherein K is equal to N.

However, Lumelsky discloses K is equal to N. (col. 5, lines 25-25)

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Atsushi, Kitagawa and Juri to include the use of K is equal to N as taught by Lumelsky in order to further conserve memory.

20. Claims 5, 21 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Atsushi, Kitagawa and Juri further in view of Pether et. al (US 6,801,925) hereinafter, Pether.

21. In regards to claim 5, Atsushi, Kitagawa and Juri differ from the claimed invention in that Atsushi and Kitagawa do not disclose wherein said bit rate converter comprises means for truncating lower significant bits of the M-bit video signal, representing the truncated lower significant bits by a different number of binary-1 's, and distributing the binary- 1's over a varying number of subsequent frames depending on the truncated lower significant bits.

However, Pether teaches a system and method for wherein said bit rate converter (fig. 5 (100)) comprises means for truncating lower significant bits (fig. 5 of the M-bit video signal (col. 3, lines 49-50), representing the truncated lower significant bits (fig. 5 “LSBs”) by a different number of binary-1 's, and distributing the binary- 1's over a varying number of subsequent frames depending on the truncated lower significant bits (fig. 5 “error”, 122 and dither col. 4, lines 1-14 of Pether).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Atsushi, Kitagawa and Juri to include the use of bit rate converter means for truncating lower significant bits of the M-bit video signal, representing the truncated lower significant bits by a different number of binary-1 's, and distributing the binary- 1's over a varying number of subsequent frames depending on the truncated lower significant bits as taught by Pether in order to provides a means of truncating bits since Pether uses error feedback and dithering to reduce visual effects as stated in (col. 1, lines 44-50 of Pether).

22. In regards to claims 21 and 23, Atsushi, Kitagawa and Juri fail to expressly teach the video process of claim 1, wherein said bit rate converter stores the selected higher N bits for a frame period and uses the stored higher N bits as higher N bits of the M-bit input video signal of a subsequent frame.

However, Pether teaches a system and method for a bit rate converter stores the selected higher N bits for a frame period and uses a stored higher N bits as higher N bits of the M-bit input video signal of a subsequent frame (col. 2, lines 20-29 fig. 5 “error”, 122 and dither col. 4, lines 1-14 of Pether).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Atsushi, Kitagawa and Juri a to include the use of a bit rate converter that stores a selected higher N bits for a frame period and uses the stored higher N bits as higher N bits of the M-bit input video signal of a subsequent frame as taught by Pether in order to provides a means of truncating bits since Pether uses error feedback and dithering to reduce visual effects as stated in (col. 1, lines 44-50 of Pether).

23. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Atsushi, Kitagawa and Juri, in view of Lu et. al (US 7,085,016) hereinafter, Lu.

24. In regards to claim 7, Atsushi, Kitagawa and Juri differ from the claimed invention in that Atsushi and Kitagawa do not explicitly disclose wherein said bit rate converter comprises means for truncating lower significant bits of the M-bit video signal so that N

bits are left in the input video signal, and dithering the N bits according to the truncated lower significant bits.

However, Lu teaches a system and method for wherein said bit rate converter comprises means for truncating lower significant bits of the M-bit video signal so that N bits are left in the input video signal, and dithering the N bits according to the truncated lower significant bits (fig. 1 col. 2, lines 57-67 of Lu).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Atsushi, Kitagawa and Juri to include the use of dithering as taught by Lu in order to use a process that selects approximate color from a mixture of other colors when transition from pixel data having high bits (M bits) to pixel data having low bits (N bits), since dithering allows for more accurately displaying graphics containing a greater range of colors than the hardware is capable of showing as stated in (col. 1, lines 15-20 of Lu).

25. In regards to claim 8, Atsushi, Kitagawa and Juri differ from the claimed invention in that Atsushi, Kitagawa and Juri do not explicitly disclose an adder for a binary-1 to higher N bits of the M-bit input video signal; a multiplexer for selecting an output of said adder or said higher N bits of the M-bit input video signal in response to a control signal; and a comparator for producing said control signal by making a comparison between lower significant bits of said M-bit input video signal and a threshold value

However, Lu teaches an adder (fig. 5 (24)) for a binary-1 to higher N bits of the M-bit input video signal; a multiplexer (fig. 5 (23)) for selecting an output of said adder or

said higher N bits of the M-bit input video signal in response to a control signal (col. 3, lines 37-60); and a comparator (fig. 5 (22)) for producing said control signal by making a comparison between lower significant bits of said M-bit input video signal and a threshold value (col. 5-6, lines 37-25).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Atsushi, Kitagawa and Juri to include the use of dithering using the particular circuit construction above as taught by Lu in order to use a process that selects approximate color from a mixture of other colors when transition from pixel data having high bits (M bits) to pixel data having low bits (N bits) since dithering allows for more accurately displaying graphics containing a greater range of colors than the hardware is capable of showing as stated in (col. 1, lines 15-20 of Lu).

Allowable Subject Matter

26. Claim 9 is allowed because the prior art does not contain a bit rate converter comprising a third frame memory for storing an output of said third multiplexer; and controller producing said first control signal only, said first and second control signals simultaneously, or said first, second and third control signals simultaneously, depending on truncated lower significant bits of the M-bit video signal.

27. Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base

claim and any intervening claims. The prior art does not contain a bit rate converter comprises: a third frame memory for storing an output of said third multiplexer; and control means for producing said first control signal only, said first and second control signals simultaneously, or said first, second and third control signals simultaneously, depending on the truncated lower significant bits.

Response to Arguments

28. Applicant's arguments with respect to claims 1-5, 7-8, and 10-23 have been considered but are moot in view of the new ground(s) of rejection.

Examiner was unable to find support for claims 20 and 22 particularly with respect to a random threshold. Examiner looked through pg 6 of the specification, lines 1-16. The only random number is in reference to the produced dot pattern.

With respect to the newly added claim limitations, a bit rate converter that adds a binary-1 to a LSB of a higher N bits of M-bits video signal is taught by Juri and Pether. It would have been obvious to one of ordinary skill in the art to incorporate these known methods in order to reduce data to save memory as stated in Juri (col. 1, lines 55-67) and to provide a method of reducing data and spreading error concealment of reduced data to subsequent data Pether (col. 2, lines 20-67) .

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to GRANT D. SITTA whose telephone number is (571)270-1542. The examiner can normally be reached on M-F 9-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on 571-272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Sumati Lefkowitz/
Supervisory Patent Examiner, Art Unit 2629

/Grant D Sitta/
Examiner, Art Unit 2629
November 3, 2009